GPIO 功能使用方法

1 適用產品：

1.1 SM59R16A2/SM59R08A2

1.2 SM59R16A5/SM59R09A5/SM59R05A5/SM59R16A3/SM59R09A3/SM59R05A3

1.3 SM59R04A2/SM59R04A1/SM59R03A1/SM59R02A1

2 以下說明僅適用：SM59R16A2/ SM59R08A2

2.1 P0 開源極之 I/O 型態[Open drain]，和標準 8051 相同。

2.2 P1~P5 皆有拉升電阻到 VDDIO，(1)當 VDDIO 浮接時，P1~P5 則視同 Open drain，(2)當 VDDIO 接至 VDD 時，P1~P5 則視同標準 51 之 I/O 型態[Quasi-bidirectional (pull-up)]。

3 以下說明適用：SM59R16A5/ SM59R09A5/ SM59R05A5/ SM59R16A3/ SM59R09A3/ SM59R05A3/ SM59R04A2/ SM59R04A1/ SM59R03A1/ SM59R02A1

可設定爲 GPIO 之對照表

原 I/O 名稱	SM59R04A2/SM59R04A1/ SM59R03A1/SM59R02A1	SM59R16A5/SM59R09A5/ SM59R05A5/SM59R16A3/ SM59R09A3/SM59R05A3
OCI_SCL	P4.4	P4.4
ALE	P4.5	P4.5
OCI_SDA	P4.6	P4.6
RESET	P4.7	P4.7
Xtal2	無	P5.4
Xtal1	無	P5.5

3.1 GPIO 使用概述：

3.2 於 40-pin PDIP 包裝最高可提供 38 個 I/O，於 44-pin PLCC and PQFP 包裝最高可提供 42 個 I/O，於 48-pin LQFP 包裝最高更可提供達 46 個 I/O 供客戶使用。(於 SM59R16A5/SM59R09A5/SM59R05A5/SM59R16A3/SM59R09A3/SM59R05A3 可多規劃出 P5.4 及 P5.5)

3.3 於特殊功能使用時(如 SPI，Two UART，IIC，KBI，CCU，PWM)，可彈性定義使用之 I/O。

3.4 每一個 I/O 可分別定義爲以下 4 種 I/O 型態之任一種：

3.4.1 標準51之I/O型態[Quasi-bidirectional (pull-up)]。

3.4.2 推挽式之I/O型態[Push-pull]。

3.4.3 僅爲輸入之I/O型態[Input only (high-impedance)]。

3.4.4 開源極之I/O型態[Open drain]。

3.5 GPIO 相關的特殊暫存器 [GPIO Special Function Register] (SFR)

For SM59R04A2/SM59R04A1/SM59R03A1/SM59R02A1 used：

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Ports											
Port 5	Port 5	D8h					P5.3	P5.2	P5.1	P5.0	0Fh
Port 4	Port 4	E8h	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh
Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh
Port 2	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								00H
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00H
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00H
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00H
P2M0	Port 2 output mode 0	D6h	P2M0[7:0]								00H
P2M1	Port 2 output mode 1	D7h	P2M1[7:0]								00H
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00H
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00H
P4M0	Port 4 output mode 0	DCh	P4M0[7:0]								00H
P4M1	Port 4 output mode 1	DDh	P4M1[7:0]								00H
P5M0	Port 5 output mode 0	DEh	-				P5M0[3:0]				00H
P5M1	Port 5 output mode 1	DFh	-				P5M1[3:0]				00H

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
AUX											
AUX	Auxiliary register	91h	BGRS	P4CC	P4SPI	P4UR1	P4IIC	P0KBI	-	DPS	00H

For SM59R16A5/SM59R09A5/SM59R05A5/SM59R16A3/SM59R09A3/SM59R05A3 used：

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Ports											
Port 5	Port 5	D8h			P5.5	P5.4	P5.3	P5.2	P5.1	P5.0	3Fh
Port 4	Port 4	E8h	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh
Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh
Port 2	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								00H
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00H
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00H
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00H
P2M0	Port 2 output mode 0	D6h	P2M0[7:0]								00H
P2M1	Port 2 output mode 1	D7h	P2M1[7:0]								00H
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00H
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00H
P4M0	Port 4 output mode 0	DCh	P4M0[7:0]								00H
P4M1	Port 4 output mode 1	DDh	P4M1[7:0]								00H
P5M0	Port 5 output mode 0	DEh	-		P5M0[5:0]						00H
P5M1	Port 5 output mode 1	DFh	-		P5M1[5:0]						00H

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
AUX & AUX2											
AUX	Auxiliary register	91h	BGRS	-	P4SPI	P4UR1	P4IIC	P0KBI	P2PWM	DPS	00H
AUX2	Auxiliary register2	92h	-	-	-	-	-	-	P42CC[1:0]		

3.6 Port 0 至 Port 5 4 種 I/O 型態選擇方式：

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

3.7 特殊功能使用之 I/O 選擇方式：

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRGS	P4CC	P4SPI	P4UR1	P4IIC	P0KBI	-	DPS	00H

P4CC: (Only SM59R04A2/SM59R04A1/SM59R03A1/SM59R02A1 have)
P4CC = 0 – Capture/Compare function on P1.

P4CC = 1 – Capture/Compare function on P4.

P4CC	CC0	CC1	CC2	CC3
0	P1.0	P1.1	P1.3	P1.4
1	P4.0	P4.1	P4.2	P4.3

P4SPI: P4SPI = 0 – SPI function on P1.
P4SPI = 1 – SPI function on P4.

P4SPI	SS	MOSI	MISO	SPI_CLK
0	P1.4	P1.5	P1.6	P1.7
1	P4.0	P4.1	P4.2	P4.3

P4UR1: P4UR1 = 0 – Serial interface 1 function on P1.
P4UR1 = 1 – Serial interface 1 function on P4.

P4UR1	RXD1	TXD1
0	P1.2	P1.3
1	P4.2	P4.3

P4IIC: P4IIC = 0 – IIC function on P1.
P4IIC = 1 – IIC function on P4.

P4IIC	IIC_SCL	IIC_SDA
0	P1.6	P1.7
1	P4.0	P4.1

P0KBI: P0KBI = 0 – KBI function on P2.
P0KBI = 1 – KBI function on P0.

P0KBI	KBI0	KBI1	KBI2	KBI3	KBI4	KBI5	KBI6	KBI7
0	P2.0	P2.1	P2.2	P2.3	P2.4	P2.5	P2.6	P2.7
1	P0.0	P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	P0.7

於 SM59R16A5/SM59R09A5/SM59R05A5/SM59R16A3/SM59R09A3/SM59R05A3 多出以下兩種：

a. PWM 可由 Port 4 輸出換到 Port 2。
b. CCU 可由 Port 1 輸出更換至 Port 2 或 Port 4。

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRGS		P4SPI	P4UR1	P4IIC	P0KBI	P2PWM	DPS	00H

P2PWM: P2PWM = 0 – PWM function on P4.

P2PWM = 1 – PWM function on P2.

P2PWM	PWM0	PWM1	PWM2	PWM3
0	P4.0	P4.1	P4.2	P4.3
1	P2.4	P2.5	P2.6	P2.7

Mnemonic: AUX2 Address: 92h

7	6	5	4	3	2	1	0	Reset
						P42CC[1: 0]		00H

P42CC[1: 0] 00: Capture/Compare function on Port1.
01: Capture/Compare function on Port2
10: Capture/Compare function on Port4
11: reserved

P42CC[1:0	CC0	CC1	CC2	CC3
00	P1.0	P1.1	P1.3	P1.4
01	P2.0	P2.1	P2.2	P2.3
10	P4.0	P4.1	P4.2	P4.3

3.8 多 4 個 GPIO 之方法：

此顆 MCU 可用 ICP 或 ISP 等燒錄模式將 OCI_SCL、ALE、OCI_SDA and RESET 等 I/O 定義成 P4.4、P4.5、P4.6 and P4.7。

各種封裝對應之 PIN 腳如下表：

	OCI_SCL/P4.4	ALE/P4.5	OCI_SDA/P4.6	RESET/P4.7
40-PIN PDIP	29	30	31	9
44-PIN PLCC	32	33	35	10
44-PIN PQFP	26	27	29	4
48-PIN LQFP	29	30	32	5

於 SM59R16A5/SM59R09A5/SM59R05A5/SM59R16A3/SM59R09A3/SM59R05A3 更可將 Xtal2 及 Xtal1 定義成 P5.4、P5.5。

各種封裝對應之 PIN 腳如下表：

	Xtal2/P5.4	Xtal1/P5.5
40-PIN PDIP	18	19
44-PIN PLCC	20	21
44-PIN PQFP	14	15
48-PIN LQFP	15	16