Product List

OB39R16A6U24,
OB39R16A6U28,
OB39R16A6U32,

Description

The OB39R16A6 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 16K-byte embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51

OB39R16A6 contains 1K+256B on-chip RAM, up to 30 GPIOs (32L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB39R16A6 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB39R16A6ihhkL
YWW
i: process identifier { U = 1.8V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

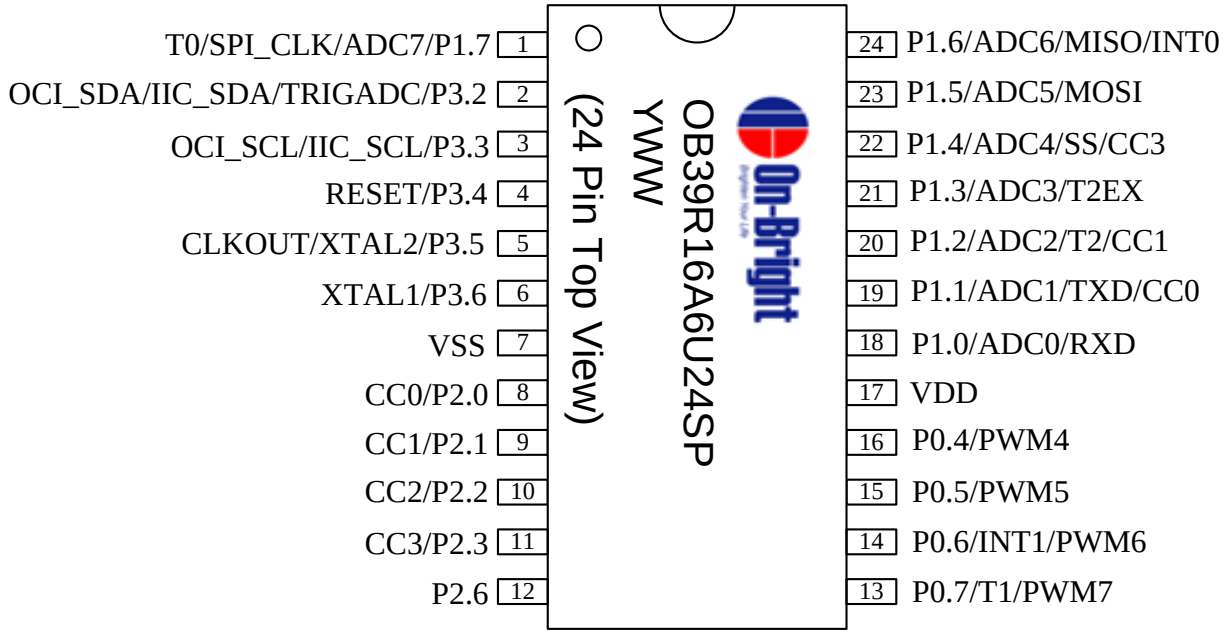
Postfix	Package
S	SOP (300 mil)
V	LQFP

Features

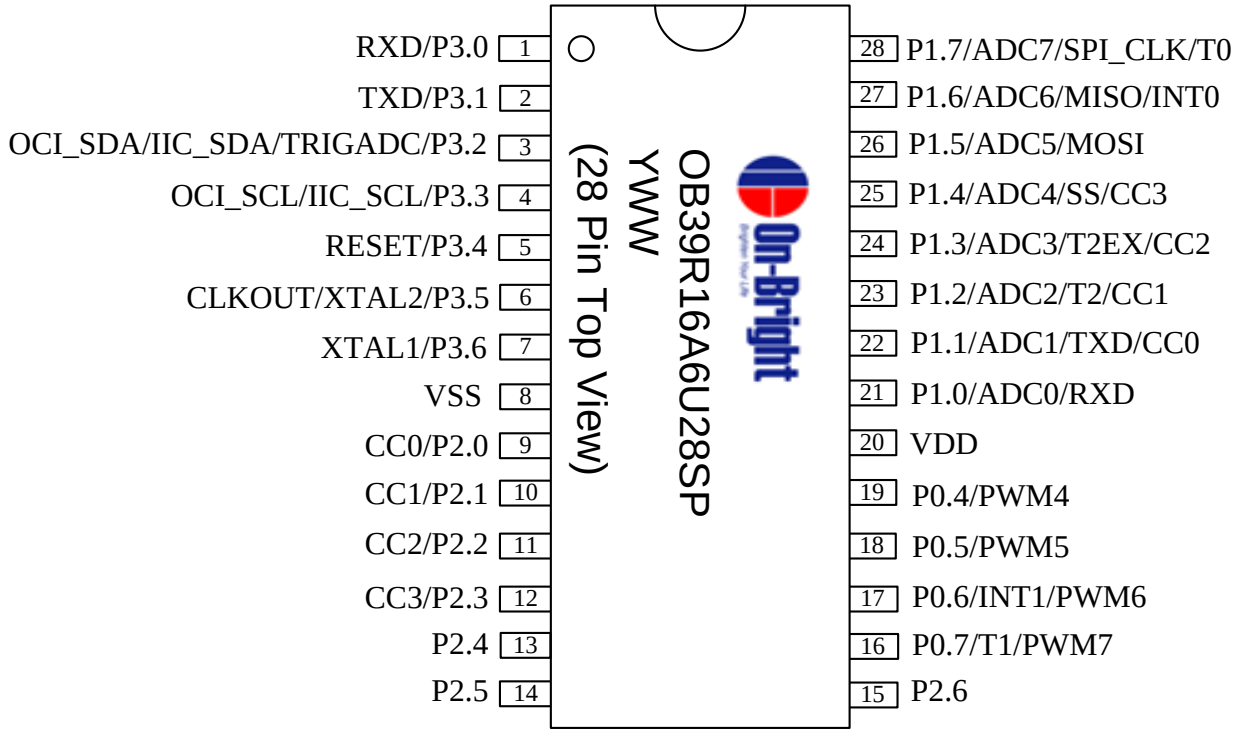
- Main Flash ROM 16KB , 128B/page
- Working voltage 1.8V~5.5V
- High speed architecture of 1 clock/machine cycle runs up to 25MHz.
- 256 bytes SRAM as standard 8052, plus 1K bytes on-chip expandable SRAM.
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- One serial peripheral interfaces in full duplex mode (UART).
  - Synchronous mode, fixed baud rate.
  - 8-bit UART mode, variable baud rate.
  - 9-bit UART mode, fixed baud rate.
  - 9-bit UART mode, variable baud rate.
- Additional Baud Rate Generator for Serial port.
- Three 16-bit Timer/Counters. (Timer 0, 1, 2).
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode).
- One SPI interface. (Master/Slave mode)
- 4-channel 14-bit PWM for motor control
- 4-channel 16-bit compare / capture / load functions.
  - Comparator out can be CCU input source internally.
  - Noise filter with CCU input with sample frequency select.
- ISP/IAP/ICP functions.
- EEPROM function.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- Fast multiplication-division unit (MDU): 16*16, 32/16, 16/16, 32-bit L/R shifting and 32-bit normalization.
- LVI/LVR (LVR deglitch 500ns).
- Enhance user code protection.
- Power management unit for IDLE and power down modes.

Pin Configuration

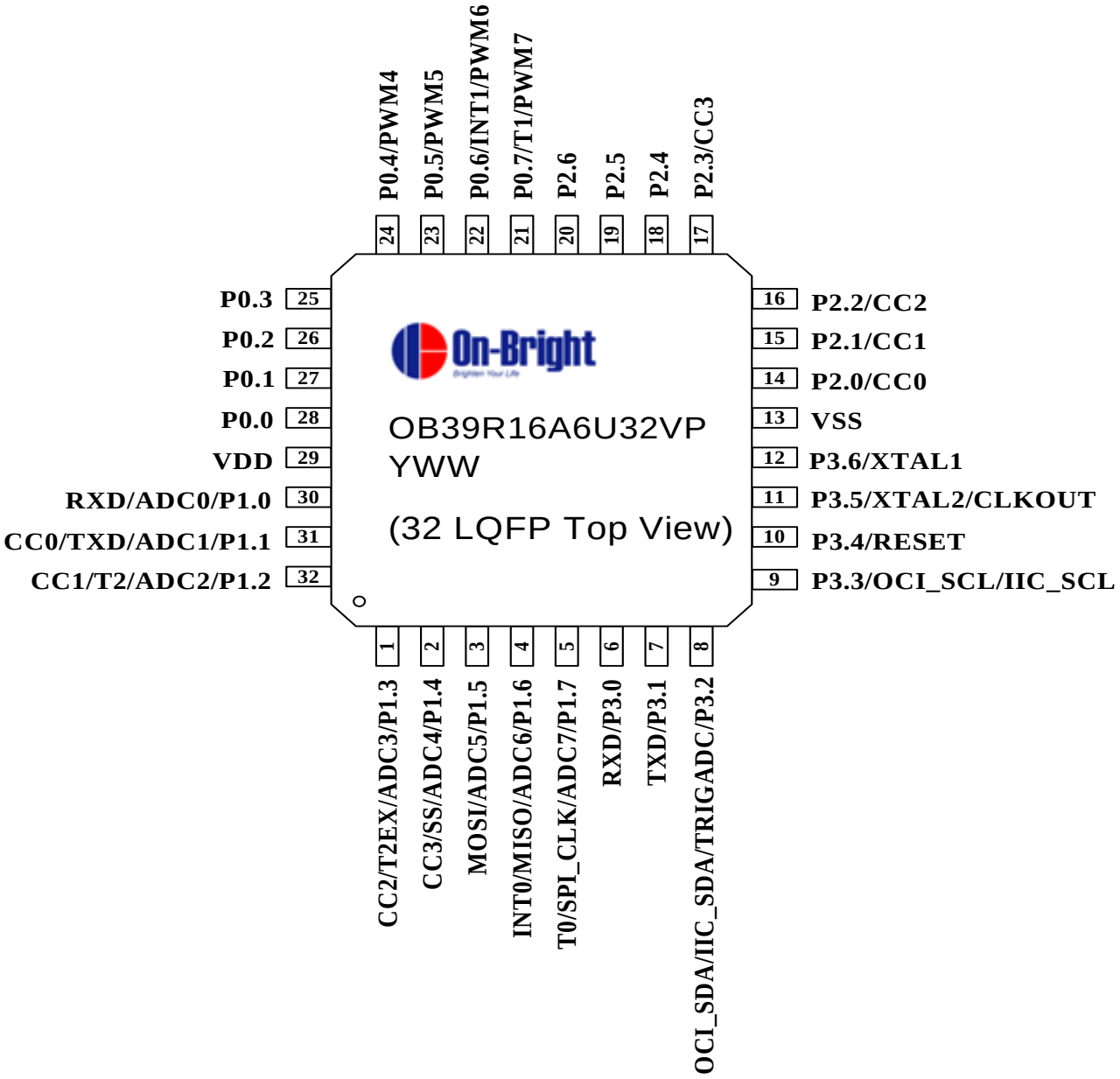
24 Pin SOP



28 Pin SOP



32 Pin LQFP



Notes：

(1) The pin Reset/P3.4 factory default is GPIO (P3.4). User can configure it to reset by a flash programmer.

(2) To avoid accidentally entering ISP-Mode(refer to section 18.4), care must be taken not asserting pulse signal at RXD P3.0 during power-up while P1.2, P1.3 or P1.4 are set to high.

(3) To apply ICP function, OCI_SDA/P3.2 and OCI_SCL/P3.3 are ICP pins during reset period. When reset finish, they are GPIO.