Product List

OB39R32T1W32VP,
OB39R32T1W28SP,
OB39R32T1W24SP,
OB39R32T1W24GP,
OB39R32T1W20SP,

Description

The OB39R32T1 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 32KB+8KB embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.

OB39R32T1 contains 768B+256B on-chip RAM, various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB39R32T1 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB39R32T1ihhkL YWW
i: process identifier { W = 2.2V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

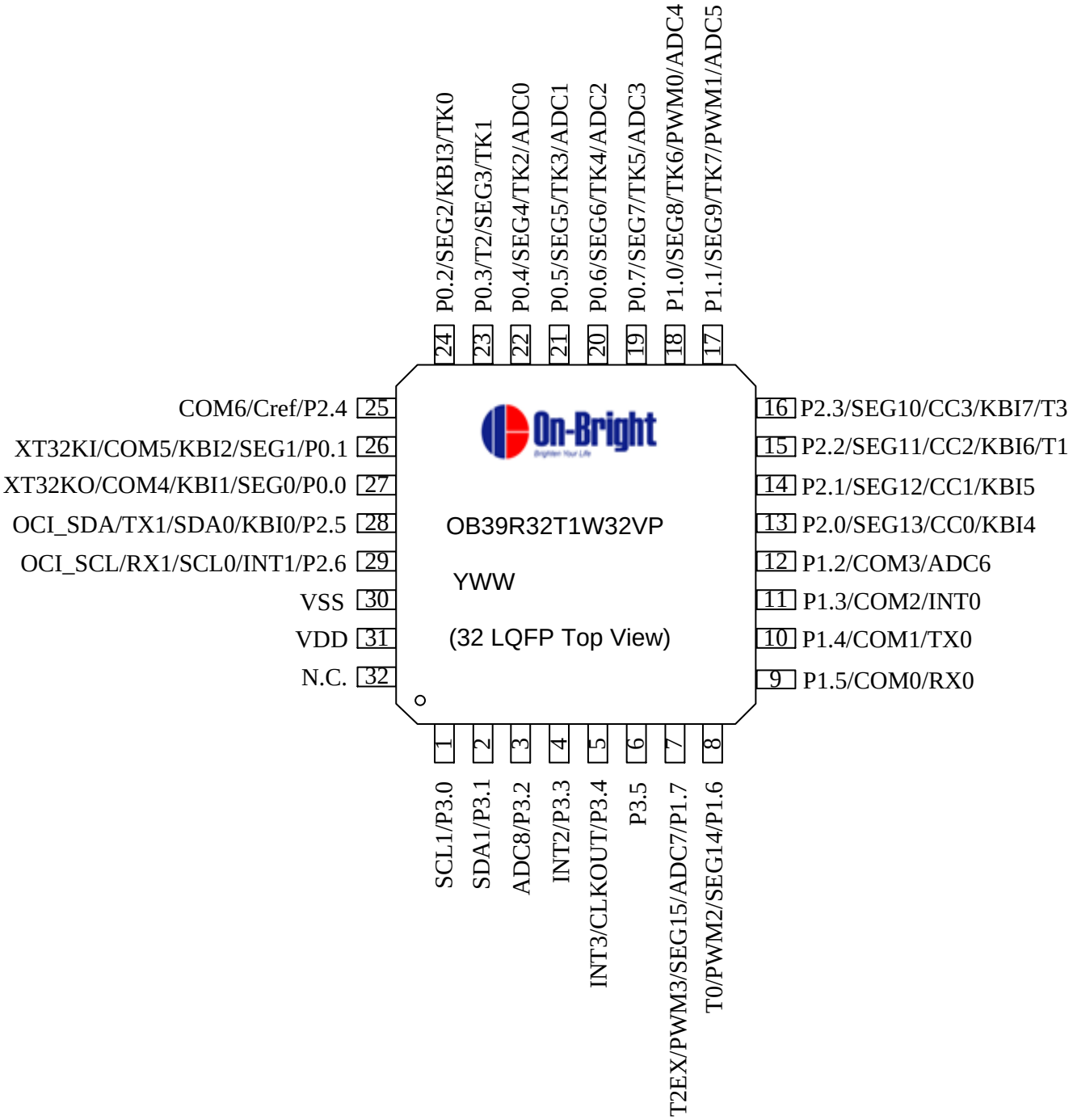
Postfix	Package
S	SOP (300 mil)
V	LQFP
G	SSOP (150 mil)

Features

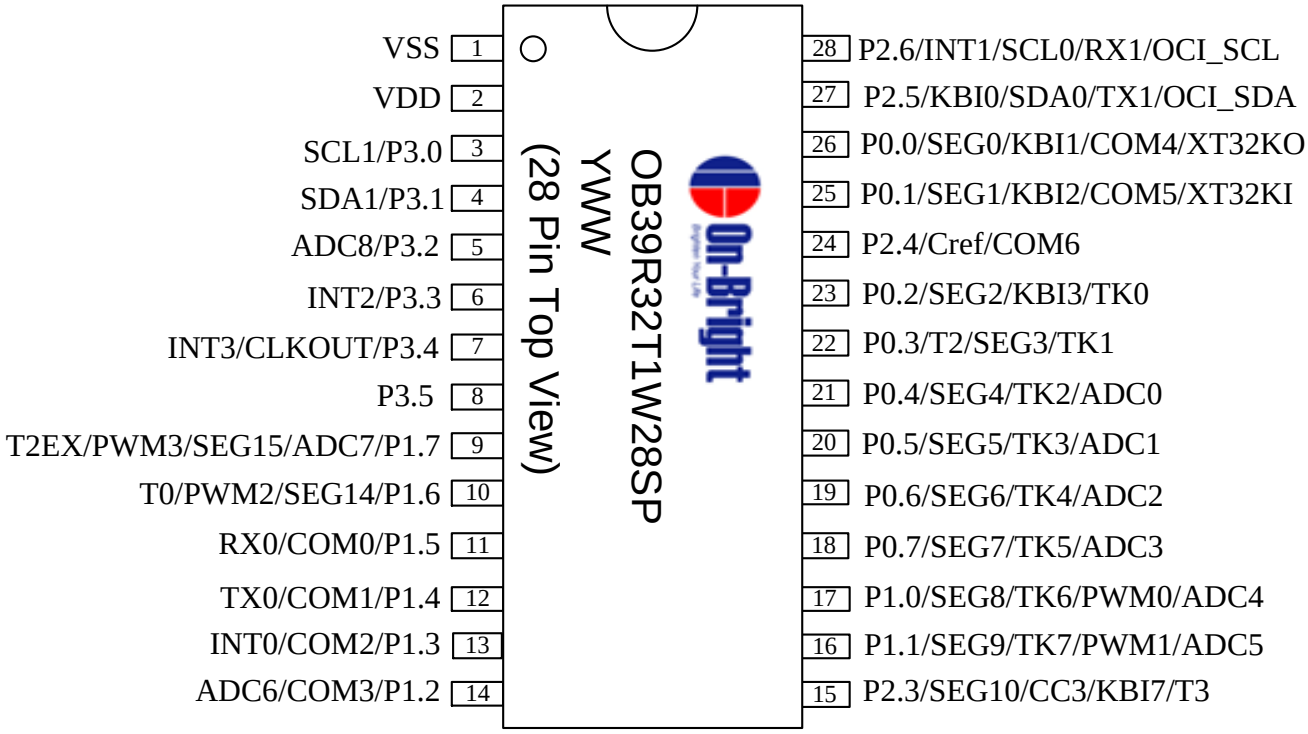
- 32KB+8KB on-chip program memory.
- Working voltage 2.2V~5.5V.
- High speed architecture of 1 clock/machine cycle runs up to 22.1184MHz.
- 1~8T can be switched on the fly.
- 256 bytes RAM as standard 8052, plus 768 bytes on-chip expandable RAM
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- Two serial peripheral interfaces in full duplex mode (UART0 & UART1)
- Up to 8 touch sense inputs, support multiplexing I/O function.
- Four 16-bit Timer/Counters. (Timer 0,1,2,3)
- Programmable watchdog reset and interrupt timer.
- Two IIC interface. (Master/Slave mode).
- 4-channel 16-bit compare / capture functions.
- 4-channel PWM.
- ISP/IAP/ICP functions.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- LVI/LVR (LVR deglitch 500ns).
- 9-channel 12-bit ADC.
- External interrupt 0, 1, 2, 3 with four priority levels.(INT x 4)
- Keyboard Interface (KBI x 8) on port 1 for eight more interrupts.
- LED driver: COM x7, Segment x 16.
- Enhance user code protection.
- Power management unit for IDLE and power down modes.

Pin Configuration

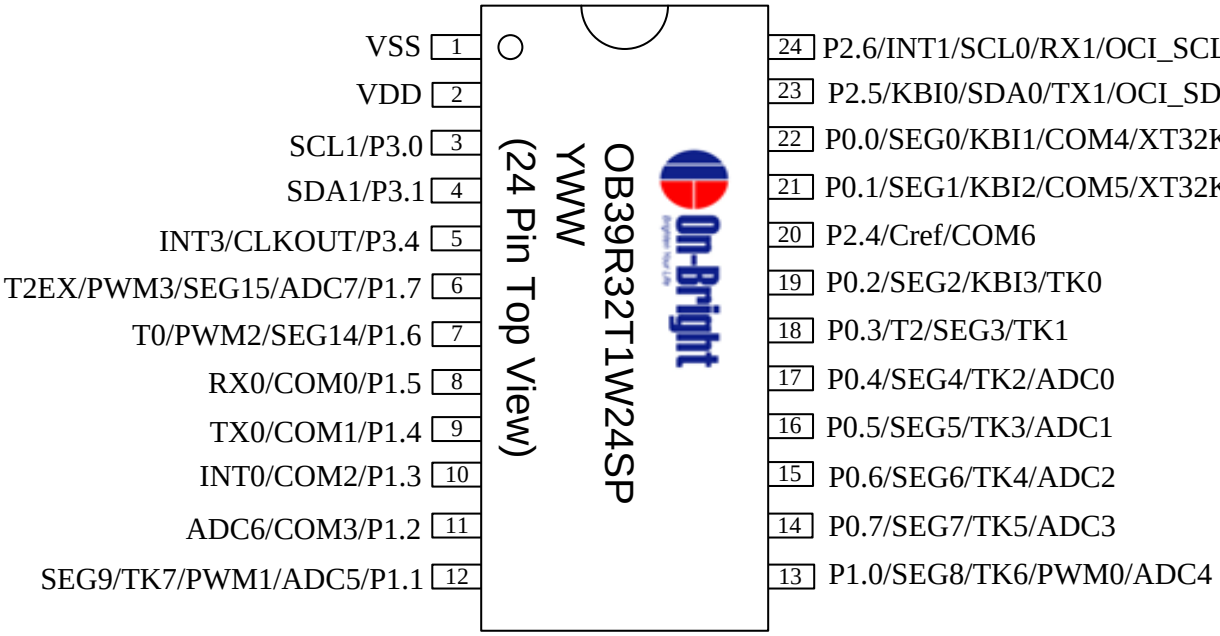
32 Pin LQFP



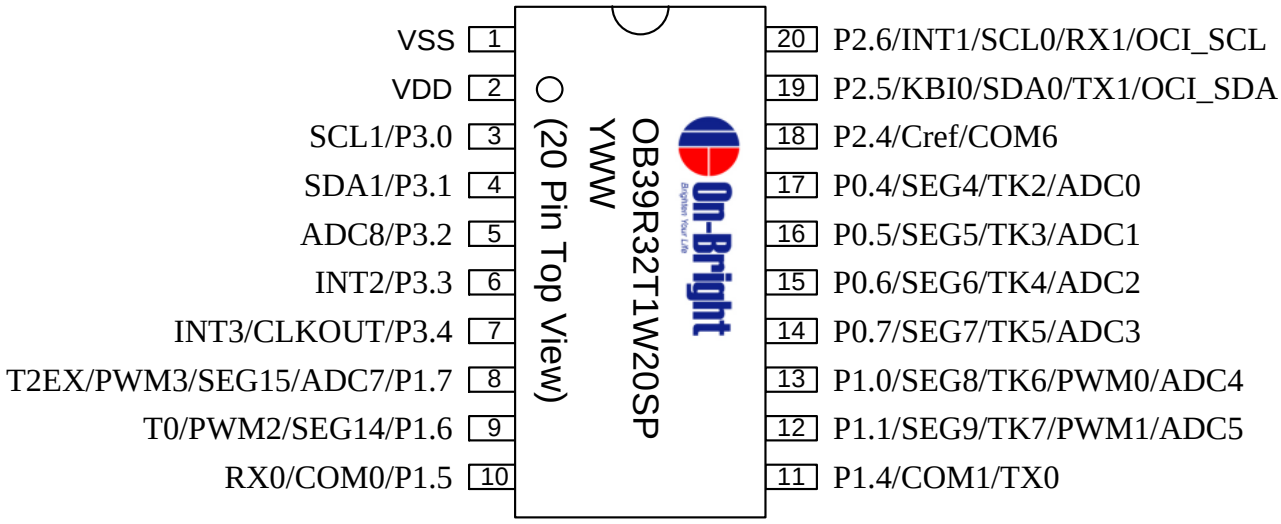
28 Pin SOP



24 Pin SOP/SSOP



20 Pin SOP



Notes：

(1) To avoid accidentally entering ISP-Mode(refer to section 19.4), care must be taken not asserting pulse signal at RXD0 P1.5 & RXD1 P2.6 during power-up while P1.6, P1.7 or P0.7 are set to high.

(2) To apply ICP function, OCI_SDA/P2.5 and OCI_SCL/P2.6 are ICP pins during reset period. When reset finish, they are GPIO.