Product List

OB39R16A3U20,
OB39R16A3U16,
OB39R16A3U14,
OB39R16A3U10,

Description

The OB39R16A3 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 16KB embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.

OB39R16A3 contains 512B on-chip RAM, up to 18 GPIOs (20L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB39R16A3 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB39R16A3 ihhkL
YWW
i：process identifier { U = 1.8V ~ 5.5V}
hh：pin count
k：package type postfix {as table below }
L：PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y： Year Code
WW：Week Code (01-52)

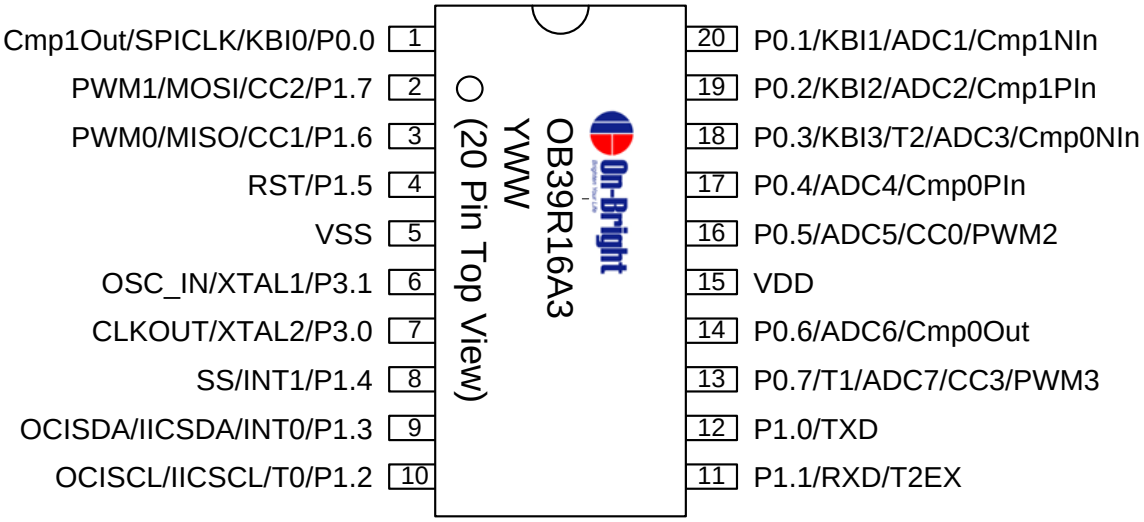
Postfix	Package
N	PDIP (300 mil)
S	SOP (300 mil)
O	SOP (150 mil)
G	SSOP (150 mil)
E	TSSOP(173mil)
B	QFN(3mm x3mm)
M	MSOP (118 mil)

Features

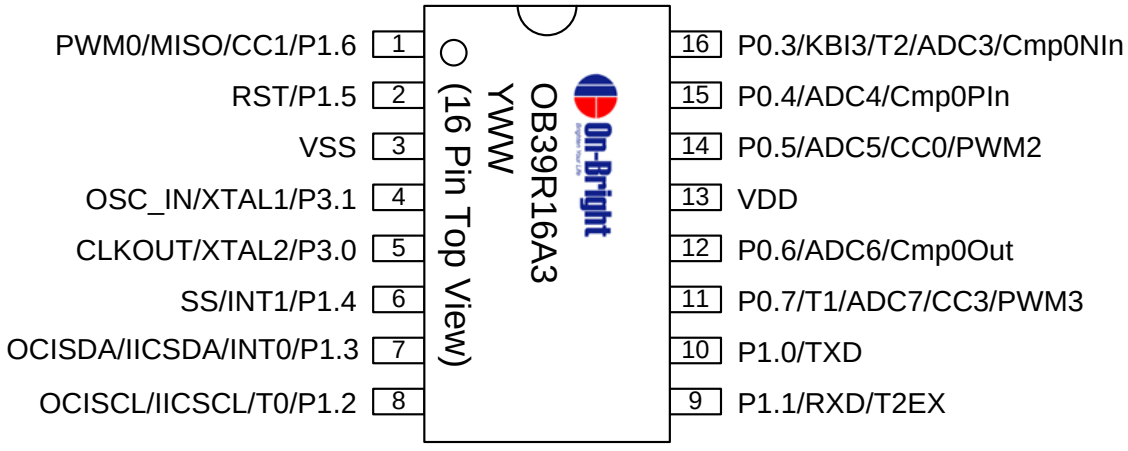
- Operating Voltage:1.8V ~ 5.5V
- High speed architecture of 1 clock/machine cycle runs up to 25MHz.
- 1~8T can be switched on the fly.
- Instruction-set compatible with MCS-51.
- 22.1184MHz Internal RC oscillator, with programmable clock divider
- 16KB on-chip program memory.
- 512B RAM as standard 8052,
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- One serial peripheral interfaces in full duplex mode.
- Additional Baud Rate Generator
- Three 16-bit Timer/Counters. (Timer 0,1,2）
- 12 ~18 GPIOs(14L ~ 20L package)
- External interrupt 0,1 with four priority levels
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode)
- One SPI interface (Master/Slave mode)
- 4-channel PWM
- 4-channel 16-bit PCA for compare(PWM) / capture / reload functions
- 7-channel 10-bit analog-to-digital converter (ADC) and 1-channel ADC0 connect to internal reference voltage
- CMP x1 Set (2 devices)
- ISP/IAP/ICP functions.
- ISP service program space configurable in N*128 byte (N=0 to 8) size.
- EEPROM function.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- Keyboard interface (KBI) for four more interrupts.
- LVI/LVR (LVR deglitch 500ns)
- IO PAD ESD over 4KV
- Enhance user code protection.
- Power management unit for IDLE and power down modes.

Pin Configuration

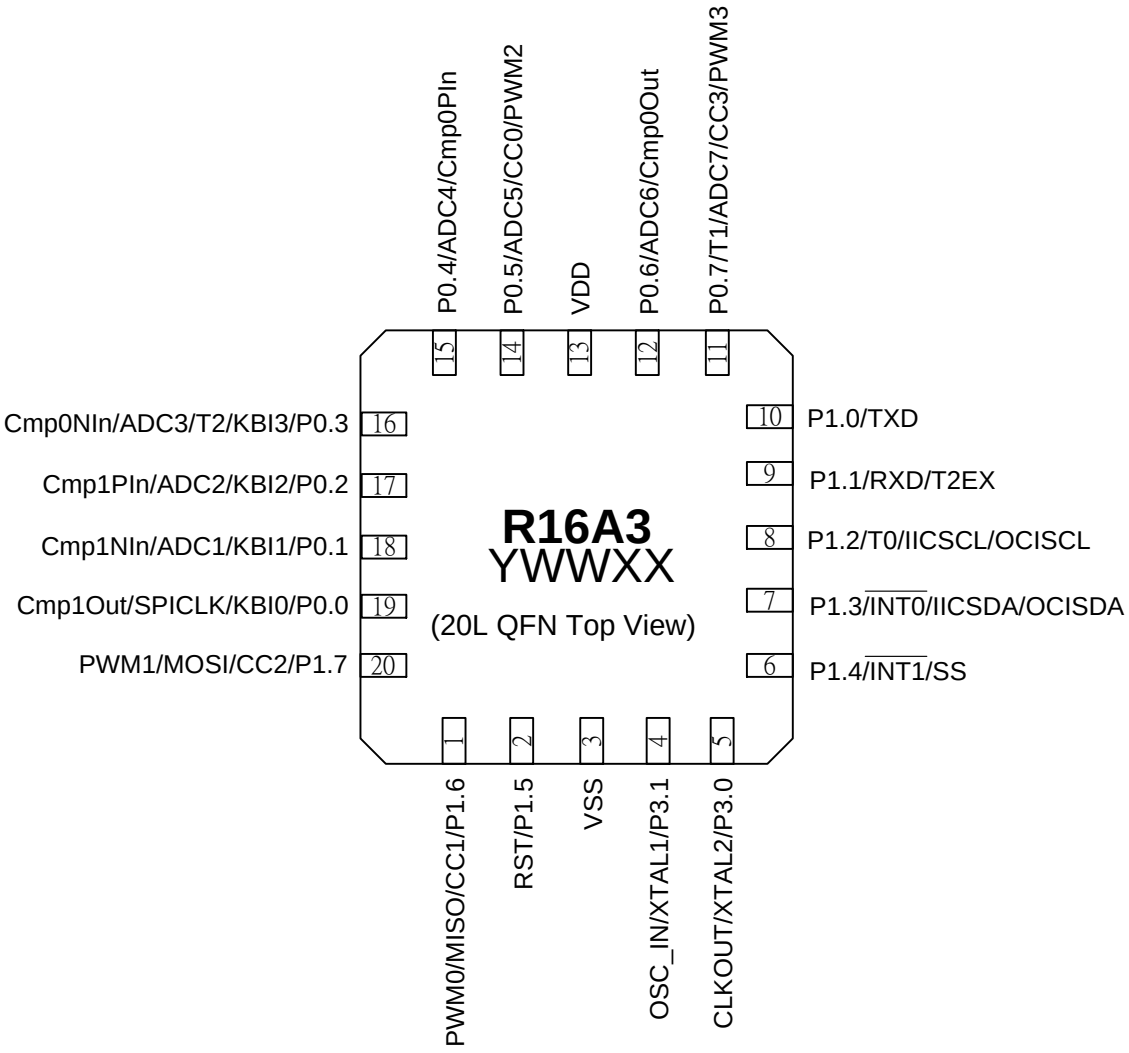
20 Pin PDIP 300mil /SOP 300mil /SSOP 150mil /TSSOP 173mil



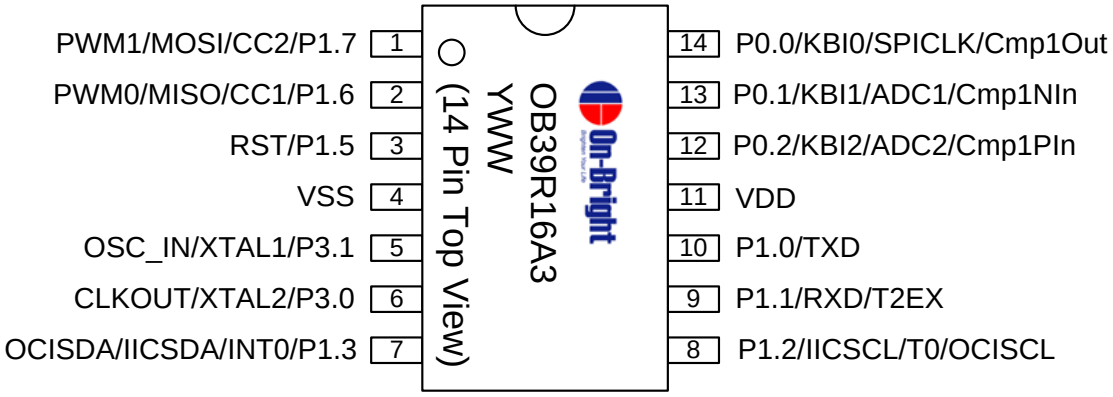
16 Pin SOP 150mil



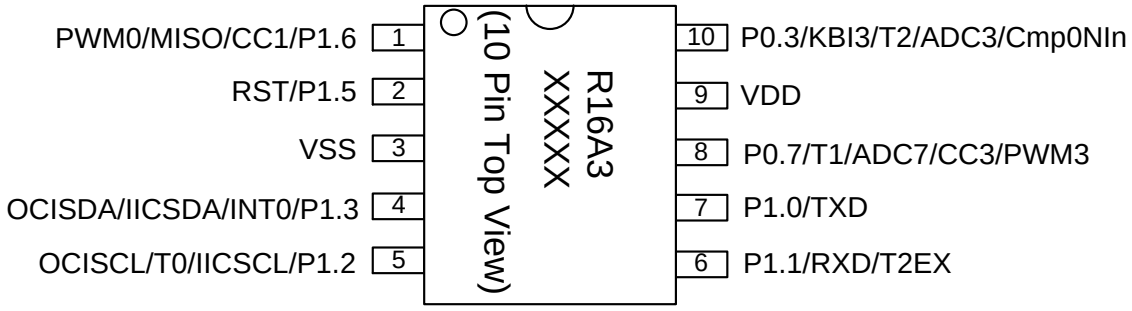
20 Pin QFN (3x3x0.75mm)



14 Pin SOP 150mil



10 Pin MSOP 118mil



Notes：

(1) The pin Reset/P1.5 factory default is GPIO (P1.5), user must keep this pin at low during power-up. User can configure it to Reset by a flash programmer.

(2) To avoid accidentally entering ISP-Mode(refer to section 18.4), care must be taken not asserting pulse signal at RXD P1.1 during power-up while P1.6 are set to high.

(3) To apply ICP function, OSI_SDA/P1.3 and OCI_SCL/P1.2 must be set to Bi-direction mode if they are configured as GPIO in system.